ABSTRACT

An output of a first data register is coupled to an input of a second data register. The same periodic clock signal clocks both data registers. A controller monitors the clock signal, a first load signal and a read signal. The controller generates a guard band signal using the clock signal and the first load signal. The controller also generates a second guard band signal from the read signal and the clock signal. A second load signal, that is used to load the second data register, is created by performing a logical AND operation on the two guard band signals.